To: Distribution
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LLRF Performance Goals for Integrated Tests at JLAB

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The planned integrated test of a LLRF control system with a superconducting cavity at JLAB will be the first opportunity to check the operation of a fully integrated system. The goals of this test are as follows:

1) (Primary Goal) Demonstrate operation of the amplitude and phase controls, implemented as I/Q control, of the cavity field:
    a. Performance of the control loop is somewhat limited by the nonstandard setup at JLAB (see below), but nevertheless, control of the cavity field during the flat-top of the pulse is expected to be better than 1% and 1°. It is likely that the SNS operational goal of 0.5% and 0.5° will be achieved.
    b. Demonstrate a reasonable settling time, from the start of the pulse to the flat-top portion. The pulse should have small overshoot (less than a few percent), and be settled to 'flat' operation in approximately 300 us.
    c. Demonstrate the ability to change the field setpoint over a reasonable range and maintain amplitude and phase control. The range of this adjustment can be determined during the test, but will likely cover settings of cavity field from approximately half the nominal desired field to approximately 25% over the nominal desired field.
2) Demonstrate operation of the cavity resonance control.
    a. Demonstrate 'cold' startup from an unknown resonance frequency to a locked frequency of 805 MHz.
    b. Demonstrate maintenance of a locked resonance of 805 MHz over a range of operating field setpoints.
3) Demonstrate both of the above performances for a long term test of at least 6 hours, with minimal shutdowns due to failures of the control system.
4) Demonstrate operation of the control system from an EPICS workstation, including the ability to monitor operation and change the operating conditions and parameters.

The above performance goals must take into consideration that the RF system and conditions under which this testing will occur are not exactly as they will be for the actual operation at Oak Ridge. The components that differ include:

1) the klystron and klystron driver (gain-bandwidth performance)
2) the RF transport system (loop delay)
3) the High Voltage system (voltage sag → RF power sag)

The high voltage system will be upgraded for this test, with the addition of capacitance to the capacitor bank. A plot from Mark Champion shows the present and expected performance of the high voltage system (Figure 1).

The droop of the upgraded bank will be close to that seen at the LANSCE accelerator. At LANSCE, the nominal trip point of the control system is 1%, 1°. In addition, modeling by Sung-il Kwon of the operation of the control system with the transport delays expected at JLAB, and significant power droop (35%) and klystron output phase change (40°), shows that good operation can be expected, primarily due to the lack of beam loading (Figure 2).

The upgraded cap bank, the experience at LANSCE, and the modeling done by Sung-il are the basis for the performance expectations given above in item 1.a.

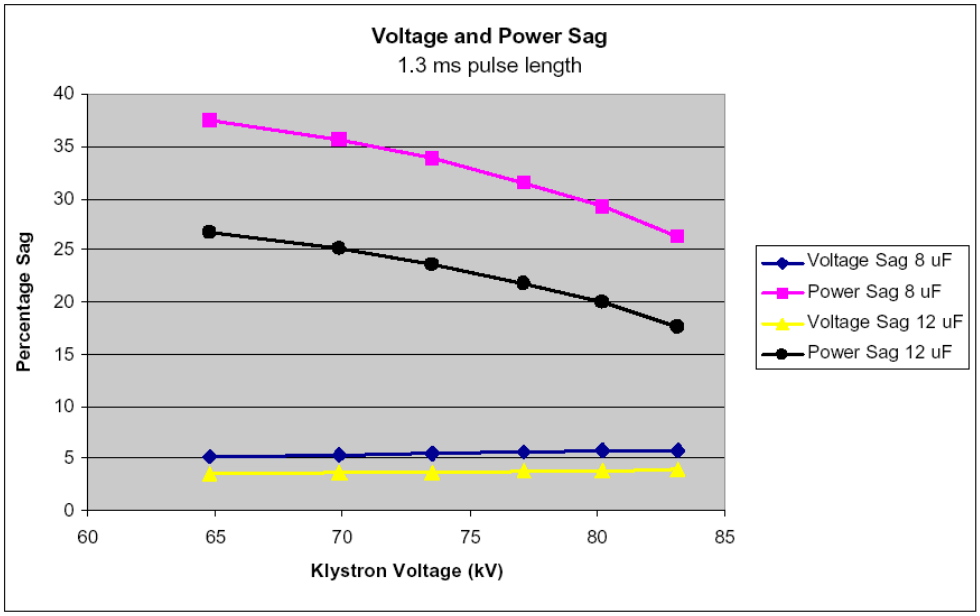

Figure 1. Voltage and power sag of the JLAB HV/RF system for existing (8 uF) and upgraded (12 uF) capacitor banks.

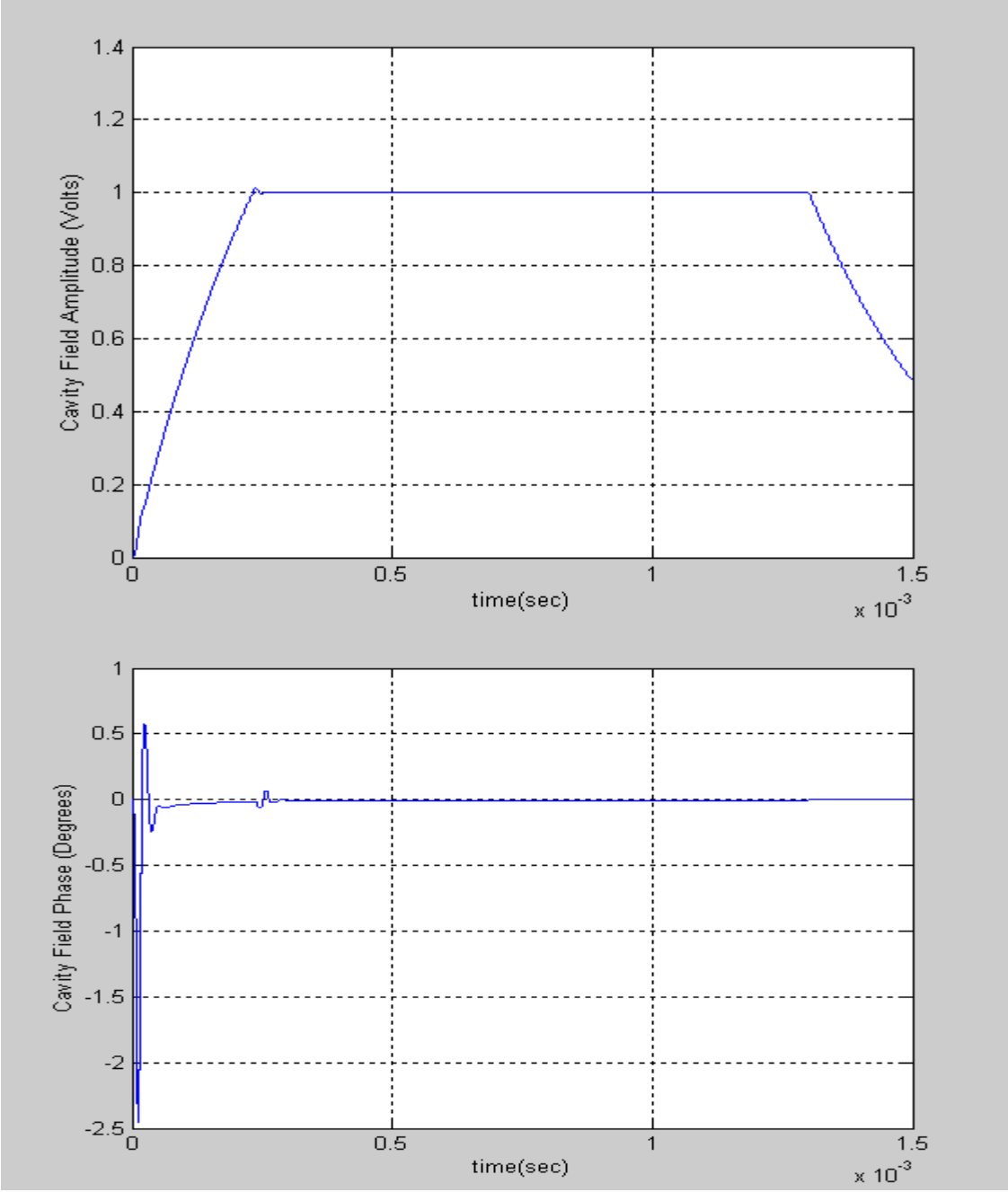

Figure 2. Modeling results of cavity field and phase under closed loop conditions with a power droop of 35% and klystron phase change of 40 degrees over the width of the pulse (with no beam loading).